AMENDMENTS TO THE CLAIMS:

Complete Claim Listing:

12. (Currently Amended) A method for forming an integrated circuit comprising:
forming a first interconnect layer over a substrate;
forming a second interconnect layer over the first interconnect layer ~~substrate~~;
depositing a passivation layer over the second interconnect layer;
forming an opening in the passivation layer that exposes a first electrical conductor of the second interconnect layer;
forming a wire bond pad that electrically connects to the first electrical conductor through the opening in the passivation layer; wherein the bond pad extends over the passivation layer and is positioned directly over a second electrical conductor ~~associated with an underlying interconnect layer selected from a group consisting of the first interconnect layer and~~ that is in the second interconnect layer, wherein the second electrical conductor is not directly attached to the wire bond pad and is electrically isolated from the wire bond pad by only the passivation layer; and
attaching a wire bond to the wire bond pad.

13. (Previously Presented) The method of claim 12 wherein the first interconnect layer includes copper.

14. (Previously Presented) The method of claim 12, wherein the second interconnect layer includes copper.

15. (Previously Presented) The method of claim 12, wherein the passivation layer is further characterized as a final passivation layer.

16. (Previously Presented) The method of claim 12, wherein the wire bond pad includes aluminum.

17. (Previously Presented) The method of claim 16, further comprising forming a barrier layer over the first electrical connector before forming the wire bond pad, wherein the barrier layer is positioned between the first electrical connector and the wire bond pad.

18. (Previously Presented) The method of claim 12, wherein the second electrical conductor is for routing power supply voltage to electrical circuits on the integrated circuit.

19. (Previously Presented) The method of claim 12, wherein a third conductor is formed using portions of the second interconnect layer and wherein the third conductor is not directly attached to the wire bond pad and routes a power supply voltage under the wire bond pad.

20. (Currently Amended) A method for forming an integrated circuit comprising attaching a wire bond to a bond pad, wherein the bond pad electrically connects to a first conductor in a final interconnect layer through an opening in a passivation layer, ~~and~~ wherein a portion of the bond pad extends over the passivation layer, and wherein the bond pad is substantially directly over a width of a second conductor in the final interconnect layer, the second conductor not directly connected to the bond pad and is electrically isolated from the bond pad by only the passivation layer.

21. (Canceled)

22. (Currently Amended) The method of claim ~~21~~ 20, wherein the wire bond is attached to the portion of the bond pad that extends over the passivation layer.

23. (Currently Amended) The method of claim 22, further comprising a ~~second~~ third electrical conductor directly underlying the portion of the bond pad that extends over the passivation layer, wherein the ~~second~~ third conductor is not directly attached to the bond pad.

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Currently Amended) A method of forming a semiconductor device comprising

forming a wire bond pad over a passivation layer that electrically connects to a first electrical conductor in a final interconnect layer through an opening in ~~a~~ the passivation layer; wherein the bond pad ~~extends over the passivation layer and~~ is positioned substantially directly over a width of a second electrical conductor ~~associated with an underlying~~ in the final interconnect layer ~~selected from a group consisting of the first interconnect layer and a second interconnect below the first interconnect layer~~, wherein the second electrical conductor is not directly attached to the wire bond pad and is electrically isolated from the wire bond pad by only the passivation layer.

28. (Currently Amended) The method of claim 27, wherein the ~~first~~ final interconnect layer includes copper.

29. (Canceled)

30. (Previously Presented) The method of claim 27, wherein the passivation layer is further characterized as a final passivation layer.

31. (Previously Presented) The method of claim 27, wherein the wire bond pad includes aluminum.